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| 浙江大学信息与电子工程学院 | 集成电路原理与设计 | 2023年10月 |
| 2023-2024学年春夏学期 |

Exercise 1

1. Consider the circuit of Fig.1.1.

a) Using the simple model with *V*Don = 0.7V, solve for *I*D;

b) Find *I*D and *V*D using the ideal diode equation. Use *I*S =10–14 A and *T*=300 K.

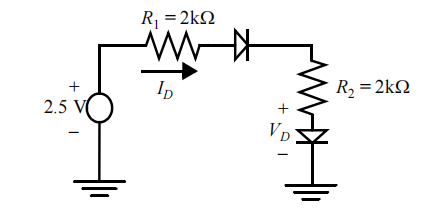


Fig.1.1

**Answer:**

1. where

iterating on this expression we can obtain

1. For the circuit in Fig.1.2, *V*s=3.3 V. Assume *A*D = 12 µm2,φ0 = 0.65 V, and m= 0.5, *N*A = 2.5×1016 and *N*D = 5×1015.

a) Is the diode forward- or reverse-biased?

b) Find *I*D and *V*D;

c) Find the depletion region width, *Wj,* of the diode;

d) Use the parallel-plate model to find the junction capacitance, *Cj*;

e) Set *Vs* = 1.5 V. Again using the parallel-plate model, explain qualitatively why *Cj* increases.

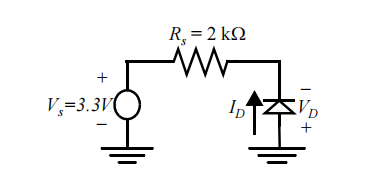


Fig.1.2

**Answer:**

1. Reverse biased
3. ,

.

.

1. *.*
2. *VSNEW* = 1.5V < *VSOLD*= 3.3V. The new voltage reduces the reverse bias of the PN junction , hence the width of the depletion region ,*Wj*, decreases. As you bring the plates of capacitor together ,the capacitance increases.
3. Fig.1.3 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the operation region (saturation, linear, or cut-off) and the drain current *ID* for each of the biasing configurations given in table. Assume the model parameters from Table.1.1, *VBS*=0 and *W/L* = 1, *L*=1um, fill the table

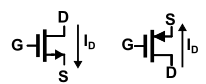


Fig.1.3

**Answer:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | *VGS*(V) | *VDS*(V) | Operation region | *ID* |
|  | 2.5 | 2.5 | saturation | 392.04uA |
| NMOS | 3.3 | 2.2 | linear | 726uA |
|  | 0.6 | 0.1 | cut-off | 0 |
|  | -0.5 | -1.25 | cut-off | 0 |
| PMOS | -2.5 | -1.8 | saturation | 176.58uA |
|  | -2.5 | -0.7 | linear | 101.5uA |

NMOS :1. Saturation *;*

2. linear *;*

3. cut-off ，

PMOS : 1. cut-off ，

2. Saturation

3. linear

1. An NMOS device is plugged into the test configuration shown below in Fig .1.4 The input *Vin* is 2V. The current source draws a constant current of 50 µA. *R* is a variable resistor between 10kΩ and 30 kΩ. Transistor M1 has following transistor parameters: *k’*= 110µV/A2, *V*T = 0.7V, and *V*DSAT = 0.6V, and has a *W/L* = 2.5µm/0.25um. For simplicity, the body effect and channel length modulation can be neglected, i.e *λ*=0, *γ*=0.

a) When *R* =10kΩ find the operation region, *VD* and *VS*.

b) For the case of *R* = 10kΩ, would *VS* increase or decrease if *λ* ≠ 0. Explain qualitatively.

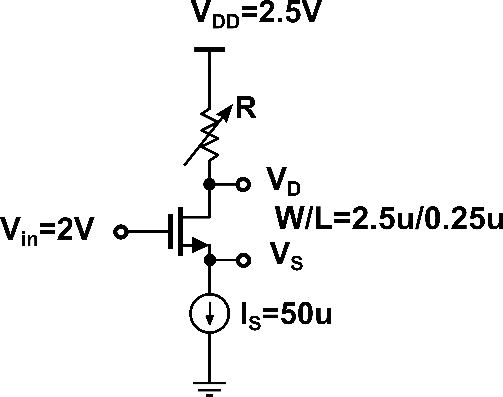


Fig.1.4

**Answer:**

**a.** When *R =10K, VD=VDD-IR=2.5-50×10-6×104=2.5-0.5=2V*.Assume the device is in saturation find *,so ,*

*.=0.913V,=1.087V* device in the saturation.

**b.** Increase. *VD*is fixed due to constant current. form would try to increase the current more then 50uA, thus needs to reduce by increase *.*

Thinking Questions(optional)

1. Show that two MOS transistors connected in parallel with channel widths of *W*1 and *W*2 and identical channel lengths of *L* can be modeled as one equivalent MOS transistor whose width is *W*1+*W*2 and whose length is *L*, as shown in Fig.1.5 Assume the transistors are identical except for their channel widths.



Fig.1.5

**Answer:**

For





……





For



Thus the equivalent length = L and the equivalent width = *W*1+ *W*2+ … + *W*n.

1. Show that two MOS transistors connected in series with channel lengths of *L*1 and *L*2 and identical channel widths of *W* can be modeled as one equivalent MOS transistor whose width is *W* and whose length is *L*1+*L*2, as shown in Fig. 1.6. Assume the transistors are identical except for their channel lengths. Ignore the body effect and channel-length modulation.



Fig.1.6

**Answer:**



(1) When *V*GS<*V*TH and *V*GE<*V*GS<*V*TH, the MOSFETs are in cut off.

(2) While M1 operates in triode (*V*DE < *V*GE –*V*THN), that is equivalent to *V*DE +*V*ES < *V*GE + *V*ES–*V*THN, i.e. *V*DS < *V*GS –*V*THN.

Thus M2 operates in triode, too.

Thus

 (1)

 (2)

Since

 (3)

 (4)

 (5)

It can be derived from equations (1), (2), (3), (4) and (5) that



So we can get 

(3) While M1 operates in saturation (*VDE* > *VGE* –*VTHN*). It means *VDE* + *VES* > *VGE*+ *VES*–*VTHN*, i.e. ***VDS* > *VGS* –*VTHN*.**

*VE* = *VG* –*VGE* < *VG* –*VTHN*, it means ***VES* < *VGS* –*VTHN。***M2 operates in triode.

So

 (1)

 (2)

 (3)

 (4)

 (5)

It can be derived from equations (1), (2), (3), (4) and (5) that



That just like a MOSFET operating in saturation, which has a length of L1+L2 and a width of W.

It can be deducted similarly that n MOSFETs in series acts as a MOSFET with an aspect ratio of W/(L1+L2+…Ln).

Table.1.1



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